



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,467	09/30/2003	Eric J. Strang	231752US6YA	2006
22850	7590	04/06/2007	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			SAXENA, AKASH	
			ART UNIT	PAPER NUMBER
			2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/06/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/673,467	STRANG, ERIC J.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above; the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 January 2007.
2a) This action is **FINAL**. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-61 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-61 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

1. Claim(s) 1-61 has/have been presented for examination based on amendment filed on 10th January 2007.
2. Claim(s) 1, 15, 20, 28, 42, 47, 55, 56 and 58 is/are amended.
3. Claim(s) 58 remain rejected under 35 USC § 101.
4. Claim(s) 1-61 remain rejected under 35 USC § 112.
5. Claim(s) 1-61 remain rejected under 35 USC § 103.
6. The arguments submitted by the applicant have been fully considered. Claims 1-61 remain rejected and this action is made FINAL. The examiner's response is as follows.

Response to Applicant's Remarks for 35 U.S.C. § 103

7. **Claims 1-21, 23, 25-48, 50 and 52-58 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Chen, further in view of Jain.**

Regarding Claims 1-21, 23, 25-48, 50 and 52-58

(Argument 1)

Applicant has pointed to section cited by examiner, Sonderman Col.9 Lines 45-61, and argued:

Sonderman Col.9 Lines 45-61

The system 100 then optimizes the simulation (described above) to find more optimal process target (Ti) for each silicon wafer, Si to be processed. These target values are then used to generate new control inputs, XTi, on the line 805 to control a subsequent process of a silicon wafer Si. The new control inputs, XTi, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like. [emphasis added]

Stating:

Thus, this section of Sonderman et al. clearly discloses that the simulation is to find a more optimum process target for each silicon wafer to be processed. The simulation results produce a new control input for the silicon wafer to be processed. Thus, Applicant respectfully submits that Sonderman et al. teach performing first principles simulation for the actual process being performed before performance of the actual process, and not the claimed performing first principles simulation for the actual process being performed during performance of the actual process. Thus, Sonderman et al. do not disclose and indeed teach away from the present invention. For at least this reason, Applicant submits that the present invention patentably defines over Sonderman et al.2

Where Sonderman does not teach the limitations:

performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed;

using the first principles simulation result obtained during the performance of the actual process to build an empirical model; and

selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool.

(Response 1)

Applicant alleges that, "Sonderman et al. teach performing first principles simulation for the actual process being performed before performance of the actual process and not the claimed performing first principles simulation for the actual process being performed during performance of the actual process." where as at the same time the claim limitation is directed to "selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool."

There seems to be two deficiencies with the argument presented above.

First the limitations themselves contradict each other. The step of "performing first principle simulation for the actual process..." seems to indicate that the simulation is happening during performance of the actual process. However the following limitation "selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool." Uses the results of the simulation to control the actual process. It is physically not possible to have the first principle simulation of the actual process to be performed at same time with actual process and then use the result to perform the actual process on the same wafer. Only one of them can be performed, whether simultaneously or using results of the simulation to feedback control the actual process from beginning.

Sonderman clearly teaches this feature at Col.9 Lines 45-61.

The second deficiency in the argument relates to Sonderman teaching away from performing concurrent simulation and actual processing. As asserted earlier, there is no such disclosure in Sonderman, and all the facts point to, contrary to applicant's assertion of teaching away, that the simulation can be performed with actual process

(Sonderman: Fig.1-3) and sequentially with feedback to the actual process for the subsequent processes/wafers (Sonderman: Col.9 Lines 45-61). Examiner finds applicant's arguments unpersuasive.

(Argument 2 & Response 2)

Further applicant has argued that Jain reference does not teach or suggest first principle simulation, as it is speculative. The claim limitation require "inputting first principle simulation model...", "performing first principle simulation..." and using "first principle simulation results...". Applicant is arguing that the cited paragraph in Jain is a proposed (not enabled) wafer scale mathematic Physical Engine (MPE) implementation proposed to solve the first principle simulation.

Examiner asserts that applicant's are arguing limitation more specifically than the claims require. Specifically, they are arguing the implementation of the first principle model, whereas none of that is claimed. The teaching of Jain clearly teaches the claimed limitation. Even if for argument sake, wafer scale implementation of the MPE engine is not enabled, the simulation concept (to perform MPE simulation of physical phenomenon) and other embodiments to implement the simulation concept (Pg. 370-372 – Sections III and IV) are disclosed. The important fact is that Jain teaches MPE to solve the physical phenomenon ranging from fluid flow to electromagnetic field dynamics to thermal patterns inside a semiconductor wafer (Abstract first line), and includes embodiments to do so. Enablement of the MPE engine in any embodiment will meet the claimed limitation. Examiner finds

applicant's argument unpersuasive and maintains the rejections for independent claims 1, 28, 55 and 58.

(Argument 3)

Applicant has argued for claim 15, that Sonderman discloses Advanced Process Control (APC) on a factory wide basis, but there is no disclosure of using network of interconnected resources inside the semiconductor device manufacturing facility to perform first principle simulation as defined in claim 21. Jain discloses interconnected resources, but they are at geographically displaced sites.

(Response 3)

Examiner finds applicant's argument unpersuasive, as there is no limitation that specifically requiring network resources not be geographically displaced. Further, even if claimed, that would be advancement on the localized resources, as it would require more technical and innovative expertise to co-ordinate such a simulation.

Secondly, in response to, Sonderman not teaching network of interconnected resources inside the semiconductor device manufacturing facility to perform first principle simulation, Jain reference is used to teach networked first principle simulation. Sonderman clearly teaches semiconductor simulation (Sonderman: Fig.1). As to interconnected resources, Sonderman states

Sonderman Col.9 Lines 58-65:

"In some embodiments, the APC can be a factory-wide software system; therefore, the control strategies taught by the present invention can be applied to virtually any of the semiconductor manufacturing tools on the factory floor"

One of ordinary skill in the art would have known that, to virtually apply control strategies to any semiconductor-manufacturing tool on the factory floor, it would require them to be networked/interconnected. Claims 15, 42 and 56 remain rejected. Applicant's argument regarding establishing a *prima facie* case of obviousness are considered and are found to be unpersuasive.

Claim Rejections - 35 USC § 112 ¶1st and response the applicant's remarks

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 1-61 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has argued that the meaning of the basic physical and chemical attribute of the semiconductor-processing tool is discernable to one of ordinary skill in the art. Although, teaching in the Maeda reference is present in exemplary format of molding tool, it is not there for a semiconductor-processing tool and does showing the physical and chemical attribute of the semiconductor-processing tool. Further, neither claim nor the disclosure presents physical and chemical attribute of the semiconductor-processing tool in form of the first principles models.

(Response to applicant's remarks)

Applicant has provided an exact support in disclosure for such attributes in the model. Applicant has incorrectly quoted specification paragraphs [0035] and [0036]. The intent seemed to be quote specification paragraphs [0037] and [0038].

These paragraph are not enabling although they rely on the commercially available packages to model the various first principle simulation models, the details of the model are absent from the specification. Examiner respectfully maintains the rejection.

Claim Rejections - 35 USC § 101 and response the applicant's remarks

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 58 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 58 discloses “computer readable medium” which is defined in the specification (Pg.32-33 [00103] Line1-9) to include tangible items (“non volatile media” and “volatile media”) and items that are non-tangible (“transmission media”). Therefore the claim as whole is not directed towards a tangible medium. One possible suggested way to overcome this rejection is to replace “computer readable medium” with “non volatile media” and “volatile media”. Transmission media (Carrier wave) is understood be non-statutory and rejected under current office practice.

(Response to applicant's remarks)

Applicant has amended “computer readable medium encoded with computer program” as curing the above deficiency because,

“a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer's functionality to be realized and is thus statutory.”

Is found to be unpersuasive because a carrier wave can still be encoded with computer program.

Response to Double Patenting

10. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,507 are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,507 (updated 9/19/06).

Application No. 10/673,467	Application No. 10/673,507
A method of controlling a process performed by a semiconductor processing tool, comprising:	A method of controlling a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attributes of the semiconductor processing tool;	inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;;
performing first principles simulation <u>for the actual process being performed</u> using the input data and the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed;	performing first principles simulation <u>for the actual process being performed</u> using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and

using the first principles simulation result to build an empirical model; and	
selecting at least one of the first principles simulation result and the empirical model to control the process performed by the semiconductor processing tool.	and using the first principles simulation result to control the <i>actual</i> process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the step of building an empirical model is inherent with the physical model. Further, both the specifications are identical in implementation and there is no difference in the implementation of the two models. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. Further the step of “selecting” which not present in the 10/673,507, is evident in the using the result to control the actual process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1-21, 23, 25-48, 50 and 52-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article “Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena” by Jain et al (Jain hereafter).

Regarding Claim 1 (Updated)

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17; Col.3 Lines 45-49) by inputting *process data relating to an actual process being performed by the semiconductor-processing tool* (Sonderman: at least in Col.3 Lines 50-67; Col.7 Lines 8-20). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed during performance of actual process* (Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63; Fig. 1-3) using the input data and the physical model to provide simulation results for the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results obtained during the performance of the actual process (Sonderman: Fig. 1-3 Col.7 Lines 4-7; Col.3 Lines 56-63) to control the *actual*

process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not explicitly teach building an empirical model and using the first principle simulation results along with the empirical model to control the process performed by the semiconductor-processing tool. Empirical model & library as understood from the specification ([0078]) is the database of the simulation results, which provides "statistically sufficient sample of the parameter space".

Chen teaches creating an empirical model as disclosed in the specification as a statistical model built based on run-to-run or batch-to-batch results and using the results to control the process performed by the semiconductor-processing tool as well as to the next simulation step (Chen: Col.3 Lines 12-47; Col.6 Lines 34-67).

Sonderman and Chen do not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and

providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; *Col.7 Lines 8-20*), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process data relating to the actual process being performed* by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process data relating to the actual process performed* by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; *Col.7 Lines 8-20*).

Regarding Claims 6-9

Sonderman teaches inputting *process data* relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at least one of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20).

Sonderman and Jain teach inputting fundamental equations as *the set of computer encoded differential equations* (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19 (Updated)

Sonderman teaches using a network of interconnected resources inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65) to perform first principle simulation (Jain: Section III) recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21 (Updated)

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent. The claim dependency is changed from claim 15 to claim 1 for claim 20.

Regarding Claim 23

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonberman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 25

Sonderman teaches inputting various parameters relating to etching, deposition etc. (Sonberman: at least in Col.5 Lines 56-67)

Regarding Claim 26

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonberman: Col.5 Lines 56-67).

Regarding Claim 27

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonberman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 28-48 (Updated)

System claims 28-48 disclose similar limitations as claims 1-21 and are rejected for the same reasons as claims 1-21 respectively.

Regarding Claim 50, 52-54

System claims 50 & 52-54 disclose similar limitations as claims 23 & 25-27 and are rejected for the same reasons as claims 23 & 25-27 respectively.

Regarding Claim 55

System claim 55 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 56 & 57 (Updated)

System claims 56 & 57 disclose similar limitations as claims 16 & 17 and are rejected for the same reasons as claims 16 & 17 respectively.

Regarding Claim 58 (Updated)

Article of Manufacture (computer program) claim 58 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 59-61(New Claims)

Jain teaches use of Navier Stokes and other known simulation solutions (reuse) for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

4. Claims 22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article “Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena” by Jain et al (Jain hereafter), further in view of IEEE article “Heat Analysis on Insulated Metal Substrates” by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of *Sonderman, Chen and Jain* are disclosed in claim 1 rejection above.

Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (*Sonderman*: at least in Col.5 Lines 62-67).

Sonderman, Chen and Jain does not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code. However, *Jain* teaches *SIMD based processing to solve the computer-encoded differential equations (Jain: Pg. 370 Section III Parallel architectures for solving PDE)*.

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (*Yunemura*: Pg. 1407 Section 1) on a silicon chip.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of *Yunemura* to *Sonderman, Chen and Jain* to create a equipment model as disclosed by *Sonderman*. The motivation to combine would have been that *Yunemura* teaches heat modeling on a

silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Yunemura's teaching thereby facilitates computer-encoded differential equations solving which is considered to be prime issue by Jain (Jain: See Section III, Networking and Dedicated MPE's for solving the computer-encoded differential equations).

Regarding Claim 49

System claim 49 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

5. Claims 24 & 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article “Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena” by Jain et al (Jain hereafter), further in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 24

Teachings of *Sonderman, Chen and Jain* are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) *but does not explicitly disclose chemical vapor and physical vapor deposition system*. Chen teaches fabrication equipment as Chemical Vapor Deposition (CVD) system (Col.5 Lines 1-5) but does not teach physical vapor deposition system. *Jain is moot on such teachings.*

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to *Sonderman, Chen and Jain*. The motivation to combine would have been that Nikoonahad and Sonderman-Chen are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35; Chen:Summary).

Regarding Claim 51

System claim 51 discloses similar limitations as claim 24 and is rejected for the same reasons as claim 24.

Conclusion

13. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner, GAU 2128
(571) 272-8351
Saturday, March 24, 2007


FRED FERRIS
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

Kamini S. Shah
Supervisory Patent Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation